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Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A circuit, comprising:

an amplifier operable to receive an input signal and a feedback signal and produce an intermediate signal; and

a variable-offset circuit operable to receive the intermediate signal and produce an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the variable-offset circuit, the amplifier being operable to reduce variation of the DC offset of the output signal by a factor that corresponds to a gain of the amplifier.

2. (Currently Amended) [The circuit of claim 1, further comprising:] A circuit, comprising:

an amplifier operable to receive an input signal and a feedback signal and produce an intermediate signal;

a variable-offset circuit operable to receive the intermediate signal and produce an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the variable-offset circuit, the amplifier being operable to reduce variation of the DC offset of the output signal; and

a correction circuit operable to receive the output signal and produce a correction signal, the correction signal being applied to the variable-offset circuit to reduce a magnitude of the DC offset of the output signal.

3. (Original) The circuit of claim 2, wherein:

the correction circuit includes,

a digital signal processor operable to measure the DC offset of the output signal and produce a control signal;

and

a digital-to-analog converter operable to receive the control signal and produce the correction signal.

4. (Original) The circuit of claim 2, wherein:

the correction signal is a current that is applied to the variable-offset circuit.

5. (Original) The circuit of claim 2, wherein:

the correction signal is a voltage that is applied to the variable-offset circuit.

6. (Original) The circuit of claim 1, wherein:

the variable-offset circuit is a variable-gain amplifier circuit and the DC offset of the output signal varies with a gain of the variable-gain amplifier.

7. (Currently Amended) [The circuit of claim 1, wherein:] A circuit, comprising:

an amplifier operable to receive an input signal and a feedback signal and produce an intermediate signal; and

a variable-offset circuit operable to receive the intermediate signal and produce an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the variable-offset circuit, the amplifier being operable to reduce variation of the DC offset of the output signal; where

the amplifier is a unity-gain buffer amplifier.

8. (Currently Amended) [The circuit of claim 1, wherein:] A circuit, comprising:

an amplifier operable to receive an input signal and a feedback signal and produce an intermediate signal; and

a variable-offset circuit operable to receive the intermediate signal and produce an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the variable-offset circuit, the amplifier being operable to reduce variation of the DC offset of the output signal; where

the circuit is compliant with one or more of the Institute of Electrical and Electronics Engineers standards 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i, 802.11n, and 802.16.

9. (Currently Amended) A circuit, comprising:

amplifying means for receiving an input signal and a feedback signal and producing an intermediate signal; and

processing means for receiving the intermediate signal and producing an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the processing means, the amplifying means being operable to reduce variation of the DC offset of the output signal by a factor that corresponds to a gain of the amplifying means.

10. (Currently Amended) [The circuit of claim 9, further comprising:] A circuit, comprising:

amplifying means for receiving an input signal and a feedback signal and producing an intermediate signal; and

processing means for receiving the intermediate signal and producing an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the processing means, the amplifying means being operable to reduce variation of the DC offset of the output signal; and

correcting means for receiving the output signal and producing a correction signal, the correction signal being used by the processing means to reduce a magnitude of the DC offset of the output signal.

11. (Original) The circuit of claim 10, wherein:

the correcting means includes,

digital signal processing means for measuring the DC offset of the output signal and producing a control signal;

and digital-to-analog conversion means for receiving the control signal and producing the correction signal.

12. (Original) The circuit of claim 10, wherein:

the correction signal is a current that is applied to the processing means.

13. (Original) The circuit of claim 10, wherein:

the correction signal is a voltage that is applied to the processing means.

14. (Original) The circuit of claim 9, wherein:

the processing means is a variable-gain amplifying means and the DC offset of the output signal varies with a gain of the variable-gain amplifying means.

15. (Currently Amended) [The circuit of claim 9, wherein:] A circuit, comprising:

amplifying means for receiving an input signal and a feedback signal and producing an intermediate signal; and

processing means for receiving the intermediate signal and producing an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the processing means, the amplifying means being operable to reduce variation of the DC offset of the output signal; where

the amplifying means is a unity-gain buffering means.

16. (Currently Amended) [The circuit of claim 9, wherein:] A circuit, comprising:

amplifying means for receiving an input signal and a feedback signal and producing an intermediate signal; and

processing means for receiving the intermediate signal and producing an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the processing means, the amplifying means being operable to reduce variation of the DC offset of the output signal; where

the circuit is compliant with one or more of the Institute of Electrical and Electronics Engineers standards 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i, 802.11n, and 802.16.

17. (Currently Amended) A wireless transceiver, comprising:

a receiver operable to receive a modulated carrier signal, the receiver including,

an amplifier operable to receive an input signal and a feedback signal and produce an intermediate signal; and

a variable-offset circuit operable to receive the intermediate signal and produce an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the variable-offset circuit, the amplifier being operable to reduce variation of the DC offset of the output signal by a factor that corresponds to a gain of the amplifier.

18. (Currently Amended) [The wireless transceiver of claim 17, wherein:] A wireless transceiver, comprising:

a receiver operable to receive a modulated carrier signal, the receiver including,

an amplifier operable to receive an input signal and a feedback signal and produce an intermediate signal;

a variable-offset circuit operable to receive the intermediate signal and produce an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the variable-offset circuit, the amplifier being operable to reduce variation of the DC offset of the output signal; and

[the receiver includes] a correction circuit operable to receive the output signal of the [output signal] variable offset circuit and produce a correction signal, the correction signal being applied to the variable-offset circuit to reduce a magnitude of the DC offset of the output signal.

19. (Original) The wireless transceiver of claim 18, wherein:

the correction circuit includes,

a digital signal processor operable to measure the DC offset of the output signal and produce a control signal;

and

a digital-to-analog converter operable to receive the control signal and produce the correction signal.

20. (Original) The wireless transceiver of claim 18, wherein:

the correction signal is a current that is applied to the variable-offset circuit.

21. (Original) The wireless transceiver of claim 18, wherein:

the correction signal is a voltage that is applied to the variable-offset circuit.

22. (Original) The wireless transceiver of claim 17, wherein:

the variable-offset circuit is a variable-gain amplifier circuit and the DC offset of the output signal varies with a gain of the variable-gain amplifier.

23. (Currently Amended) [The wireless transceiver of claim 17, wherein:] A wireless transceiver, comprising:

a receiver operable to receive a modulated carrier signal, the receiver including,

an amplifier operable to receive an input signal and a feedback signal and produce an intermediate signal; and

a variable-offset circuit operable to receive the intermediate signal and produce an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the variable-offset circuit, the amplifier being operable to reduce variation of the DC offset of the output signal; where

the amplifier is a unity-gain buffer amplifier.

24. (Currently Amended) [The wireless transceiver of claim 17, wherein:] A wireless transceiver, comprising:

a receiver operable to receive a modulated carrier signal, the receiver including,

an amplifier operable to receive an input signal and a feedback signal and produce an intermediate signal; and

a variable-offset circuit operable to receive the intermediate signal and produce an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the variable-offset circuit, the amplifier being operable to reduce variation of the DC offset of the output signal; where

the wireless transceiver is compliant with one or more of the Institute of Electrical and Electronics Engineers standards 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i, 802.11n, and 802.16.

25. (Currently Amended) A wireless transceiver, comprising:

receiver means for receiving a modulated carrier signal,

the receiver means including,

amplifying means for receiving an input signal and a feedback signal and producing an intermediate signal; and

processing means for receiving the intermediate signal and producing an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the processing means, the amplifying means being operable to reduce variation of the DC offset of the output signal by a factor that corresponds to a gain of the amplifying means.

26. (Currently Amended) [The wireless transceiver of claim 25, wherein:] A wireless transceiver, comprising:

receiver means for receiving a modulated carrier signal,

the receiver means including,

amplifying means for receiving an input signal and a feedback signal and producing an intermediate signal;

processing means for receiving the intermediate signal and producing an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the processing means, the amplifying means being operable to reduce variation of the DC offset of the output signal; and

[the receiver means includes] correcting means for receiving the output signal and producing a correction signal, the correction signal being used by the processing means to reduce a magnitude of the DC offset of the output signal.

27. (Original) The wireless transceiver of claim 26, wherein:

the correcting means includes,

digital signal processing means for measuring the DC offset of the output signal and producing a control signal;

and

digital-to-analog conversion means for receiving the control signal and producing the correction signal.

28. (Original) The wireless transceiver of claim 26, wherein:

the correction signal is a current that is applied to the processing means.

29. (Original) The wireless transceiver of claim 26, wherein:

the correction signal is a voltage that is applied to the processing means.

30. (Original) The wireless transceiver of claim 25, wherein:

the processing means is a variable-gain amplifying means and the DC offset of the output signal varies with a gain of the variable-gain amplifying means.

31. (Currently Amended) [The wireless transceiver of claim 25, wherein:] A wireless transceiver, comprising:

receiver means for receiving a modulated carrier signal,

the receiver means including,

amplifying means for receiving an input signal and a feedback signal and producing an intermediate signal; and

processing means for receiving the intermediate signal and producing an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the processing means, the amplifying means being operable to reduce variation of the DC offset of the output signal; where

the amplifying means is a unity-gain buffering means.

32. (Currently Amended) [The wireless transceiver of claim 25, wherein:] A wireless transceiver, comprising:

receiver means for receiving a modulated carrier signal,

the receiver means including,

amplifying means for receiving an input signal and a feedback signal and producing an intermediate signal; and

processing means for receiving the intermediate signal and producing an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the processing means, the amplifying means being operable to reduce variation of the DC offset of the output signal; where

the wireless transceiver is compliant with one or more of the Institute of Electrical and Electronics Engineers standards 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i, 802.11n, and 802.16.

33. (Currently Amended) A method for reducing variation of a DC offset, the method comprising:

amplifying an input signal to produce an intermediate signal;

processing the intermediate signal to produce a feedback signal and an output signal, the output signal having a DC offset that varies corresponding to a varying parameter of circuitry used to process the intermediate signal; and

reducing variation of the DC offset of the output signal using the feedback signal by a factor that corresponds to a gain of the amplification.

34. (Currently Amended) [The method of claim 33, further comprising:] A method for reducing variation of a DC offset, the method comprising:

amplifying an input signal to produce an intermediate signal;

processing the intermediate signal to produce a feedback signal and an output signal, the output signal having a DC offset that varies corresponding to a varying parameter of circuitry used to process the intermediate signal;

reducing variation of the DC offset of the output signal using the feedback signal;

measuring the DC offset of the output signal; and

applying a correction signal to the circuitry used to process the intermediate signal to reduce a magnitude of the DC offset of the output signal.

35. (Original) The method of claim 34, wherein:

measuring the DC offset includes digitally measuring the DC offset; and

applying a correction signal includes applying an analog correction signal produced responsive to a digital control signal, the digital control signal produced responsive to the digital measurement of the DC offset.

36. (Original) The method of claim 34, wherein:

applying a correction signal includes applying a correction current.

37. (Original) The method of claim 34, wherein:

applying a correction signal includes applying a correction voltage.

38. (Original) The method of claim 33, wherein:

processing the intermediate signal includes variably amplifying the intermediate signal; and

the DC offset of the output signal varies with a variation of the variable amplification.

39. (Currently Amended) [The method of claim 33, wherein:] A method for reducing variation of a DC offset, the method comprising:

applifying an input signal to produce an intermediate signal;

processing the intermediate signal to produce a feedback signal and an output signal, the output signal having a DC offset that varies corresponding to a varying parameter of circuitry used to process the intermediate signal;

reducing variation of the DC offset of the output signal using the feedback signal; and

amplifying the input signal includes buffering the input signal.

40. (Currently Amended) [The method of claim 33, wherein:] A method for reducing variation of a DC offset, the method comprising:

amplifying an input signal to produce an intermediate signal;

processing the intermediate signal to produce a feedback signal and an output signal, the output signal having a DC offset that varies corresponding to a varying parameter of circuitry used to process the intermediate signal; and

reducing variation of the DC offset of the output signal using the feedback signal; where

the method is compliant with one or more of the Institute of Electrical and Electronics Engineers standards 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i, 802.11n, and 802.16.